REMARKS

The Examiner rejected claims 1-32 under 35 U.S.C. 103(a) as being unpatentable over Radjassamy (U.S. PN: 6,331,800) in view of Tsukamoto et al. (U.S. PN: 5,930,269).

Applicants respectfully traverse the §103(a) rejections with the following arguments:

35 USC § 103 Rejections

As to claims 1 and 6, the Examiner states that "Radjassamy in figure 3 disclose or teach an integrated circuit comprising a first latch (302) coupled to first clock signal (CK1N) and first logic (304), second latch (306) coupled to second clock signal (CK2N) and second logic (308) for adjusting of clock edge rise/fall times between non-overlapping clock signals and thereby climinate a race (see col. 1, lines 5-9). Further, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Radjassamy **do not explicitly** show or teach power (rails) applied separetly to each of the IC chips wherein each IC chips comprise latches and logic circuits. **However**, Tsukamoto et al. in figure 4 teach a testing system comprises a burn-in board (11) to be diagnosed, a control signal generator (12) includes clock generator (12a) generates a clock signal CLK, and supplies the clock signal CLK to the burn-in board via scan signal distributor (12b), a power distributor (13) for supplying electric power Vcc to the burn-in board and in figure 5 the burn-in board shows products (IC1 1/IC12/IC1n, IC21/IC22/IC2n...) of a semiconductor integrated circuit device arranged in rows

and columns on the burn-in board, and are electrically connected through contact pins and furthermore Power supply lines VCC1, VCC2 and VCCm (power rails) are respectively associated with the columns of products of semiconductor device and the products are powered with power potential Vcc and the ground potential supplied from the associated power supply lines VCC1 to VCCm (see col. 3, lines 55-67 and col. 4, lines 1-22). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Radjassamy to include power supplies for powering clocks and latches as taught by Tsukamoto et al. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to diagnosis the products on the burn-in board without undesirable influence of a partially defective product and automatically classifies the products between the excellent group, the partially defective group an the defective group (see col. 9, lines 48-58)."

First, Applicants maintain that Tsukamoto et al. does not show all features required to combine Tsukamoto et al. with Rajassamy. Specifically, Tsukamoto et al. does not show any latches or logic circuits (or stages) connected to power supplies VCC1-VCCm. Tsukamoto et al. teaches only VCC1-VCCm powering different integrated circuits (see Tsukamoto et al. FIG. 5), There is no disclosure in Tsukamoto et al. that these integrated circuits contain latches no less how latches would be wired to the power supplies.

Second, Applicants contend that there is no motivation to modify Rajassamy with Tsukamoto et al. as the method used by Tsukamoto et al. when applied to Rajassamy does not result in the benefit stated. Applicants respectfully point out that Radjassamy is directed to a serial test method while Tsukamoto et al. is directed to a parallel test method (see Tsukamoto FIG. 5). The Examiner states that the motivation to modify Rajassamy with Tsukamoto et al. is

"in order to diagnosis the products on the burn-in board without undesirable influence of a partially defective product and automatically classifies the products between the excellent group, the partially defective group an the defective group" The "undesirable influence" of Tsukamoto et al. is a power supply short to ground on a damaged I/O pin of one IC interacting with the signal generated on I/O pins of other I/Cs when the I/O pins of all ICs are coupled in parallel to a common data line (see and col. 2, lines 33-59). The logic circuits of Rajassamy are connected in series (see Rajassamy FIG. 3 and col. 1, lines 28-30). Rajassamy specifically tests for faults in a logic pattern clocked serially and a fault on one logic stage will propagate through all logic stages regardless of how power is supplied to the logic stages or latches of Rajassamy.

Based on the preceding arguments, Applicants respectfully maintain that claims 1 and 6 are not unpatentable over Radjassamy in view of Tsinker and are in condition for allowance. Since claims 2-5 depend from claim 1, and claims 7-10 depend from claim 6, Applicants respectfully maintain that claims 2-5 and 7-10 are likewise in condition for allowance.

As to claims 11-16, the Examiner states "Radjassamy substantially teach or disclose an integrated circuit comprising clocked logic gates a method for increasing the rise/fall of clock edges in an IC commencing with the identification (detecting) of a clock signal with a clock edge having a poor rise/fall time (see abstract and col. 3, lines 34-43). Further, Radjassamy in figure 3, disclose first latch (302) coupled to first clock signal (CK1N) and first logic (304), second latch (306) coupled to second clock signal (CK2N) and second logic (308). Furthermore, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall

time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Radjassamy **do not explicitly** show or teach power (rails) applied separately to each of the IC chips wherein each IC chips comprise latches and logic circuits. **However,** Tsukamoto et al. in figure 4 teach a testing system comprises a burn-in board (11) to be diagnosed, a control signal generator (12) includes clock generator (12a) generates a clock signal CLK, and supplies the clock signal CLK to the burn-in board via scan signal distributor (12b), a power distributor (13) for supplying electric power Vcc to the burn-in board and in figure 5 the burn-in board shows products (ICI 1/IC12/ICln, IC21/IC22/IC2n...) of a semiconductor integrated circuit device arranged in rows and columns on the burn-in board, and are electrically connected through contact pins and furthermore Power supply lines VCC1, VCC2 and VCCm (power rails) are respectively associated with the columns of products of semiconductor device and the products are powered with power potential Vcc and the ground potential supplied from the associated power supply lines VCC1 to VCCm (see col. 3, lines 55-67 and col. 4, lines 1-22). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Radjassamy to include power supplies for powering clocks and latches as taught by Tsukamoto et al. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to diagnosis the products on the burn-in board without undesirable influence of a partially defective product and automatically classifies the products between the excellent group, the partially defective group an the defective group (see col. 9, lines 48-58)."

Applicants note that claim 11includes all the elements of claim 1 and additionally adds limitations related to third and fourth power rails and that the Examiners stated reasons for rejecting claim 11is essentially identical to those given for rejecting claim 1. Therefore

Applicants contend all of Applicants' arguments *supra* in respect to claims 1 and 6 are applicable to claim 11. Based on the preceding arguments, Applicants respectfully maintain that claim 11 is are not unpatentable over Radjassamy in view of Tsukamoto et al. and is in condition for allowance. Since claims 12-16 depend from claim 11, Applicants respectfully maintain that claims 12-16 are likewise in condition for allowance.

As to claims 17 and 22, the Examiner states "method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Furthermore, Tsukamoto et al. teach a testing system selectively activates products of a semiconductor integrated circuit device mounted on a burn-in board and a power distributor incorporated in the testing system supplies electric power only to the activated products so that non-activated products do not affect the test data signals (see abstract)."

Applicants contend all of Applicants' arguments *supra* in respect to claims 1 and 6 are applicable to claims 17 and 22. Based on the preceding arguments, Applicants respectfully maintain that claims 17 and 22 are not unpatentable over Radjassamy in view of Tsukamoto et al. and are in condition for allowance. Since claims 18-21 depend from claim 17 and claims 23-26 depend from claim 22, Applicants respectfully maintain that claims 18-21 and 23-26 are likewise in condition for allowance.

As to claims 27-32 the Examiner states that "As per claims 27-32, Radjassamy in view of Tsukamoto et al. teach or disclose all the subject matter claimed in claim 11, including

Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Furthermore, Tsukamoto et al. teach a testing system selectively activates products of a semiconductor integrated circuit device mounted on a burn-_in board and a power distributor incorporated in the testing system supplies electric power only to the activated products so that non-activated products do not affect the test data signals (see abstract)."

Applicants contend that Applicants' arguments given *supra* in respect to claims 1 and 6 are applicable to claim 27. Based on the preceding arguments, Applicants respectfully maintain that claims 27 is not unpatentable over Radjassamy in view of Tsukamoto et al. and is in condition for allowance. Since claims 28-32 depend from claim 27, Applicants respectfully maintain that claims 28-32 are likewise not unpatentable over Radjassamy in view of Tsukamoto et al. and are in condition for allowance.

Applicants contend that claims 3, 8, 13, 19 and 24 are not obvious in view of Radjassamy in view of Tsukamoto et al. because Radjassamy in view of Tsukamoto et al. does not teach or suggest every feature of claims 3, 8, 13, 19 and 24.

Using claim 1 as an example, the Examiner states "Radjassamy in view of Tsukamoto et al. teach all the subject matter claimed in claims 1 and 6 including Tsukamoto et al. in figure 5 teach plurality of burn-in products whereby each of the products connected by separate clocks (SCN1, SCN2...) and voltage lines VCC1, VCC2...)."

Applicants maintain, in the case of claim 3, Radjassamy in view of Tsukamoto et al. does not teach or suggest "said first and second clocks powered from a third power rail." Applicants point out that claim 3 specifically teach the clocks being powered from a different power supply than the power supply powering the latches and logic circuits. Rajassamy and Tsukamoto et al. are silent as to the source of the power for their clocks.

Applicants believe that the argument present for claim 3 is applicable to the Examiners rejection of claims 8, 13, 19 and 24 as well and based on the preceding argument for claim 3, Applicants respectfully maintain that claims 3, 8, 13, 19 and 24 are not unpatentable over Radjassamy in view of Tsukamoto et al.and are in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 1-32 meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below.

Respectfully submitted,
FOR:

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